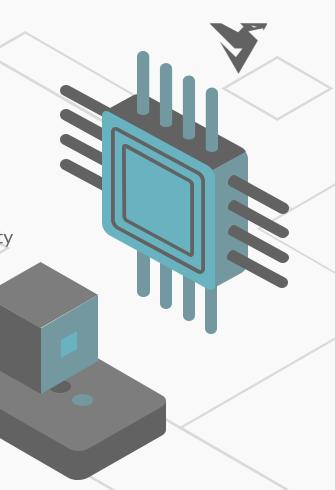


## Don't trust us... Trust facts

- ~70% of all cyberattacks are due to a lack of memory safety.
- A new hardware chip design, CHERI, completely removes these issues due to new hardware chip design.
- By utilising capabilities instead of pointers, robust memory integrity without interference is guaranteed.
- CHERI-enabled processors can run existing legacy code with eat
- Relying on CHERI hardware ensures no software backdoor automatically rejecting dangerous code.



# CHERI Alliance Our Key Partners







### Google

A founding member of the CHERI alliance with a foot in a wide range of industries.



### Siemens

Siemens is a full member of the CHERI alliance and a key player in the automotive industry.



### **University of Cambridge**

University of Cambridge is a forerunner of research in CHERI. We use UoC rocket chips within WARP.



#### NCSC

We aim to have WARP used in critical national infrastructure for sovereign benefit.

## CHERI Alliance Non-member backers







#### **ARM**

ARM is one of the most prominent leaders in research of CHERI based devices.



#### **DARPA**

"the agency that shaped the modern world", DARPA initially funded the research into CHERI back in 2010.



#### Microsoft

Developer of hardware, software and cloud services, Microsoft has expressed public interest in the future of CHERI devices.



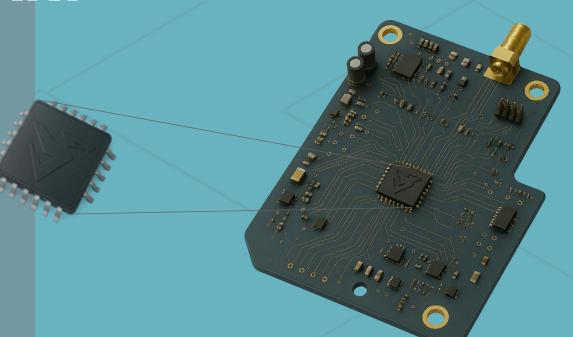
#### **UKRI**

UK Research and Innovation has invested in many project relating to advancing CHERI.

WYVERN ADVANCED RISC-V PROCESSOR

## WARP





### WYVERN ADVANCED RISC-V PROCESSOR

### What is WARP?







### **CHERI** native

Eliminates 70% of IP and memory vulnerabilities by design; like preventing a car crash by flying.



### **RISC-V** sovereign

Mitigates reliance on closed ecosystems and ARM processors.



### Secure by Design

Vulnerabilities are prevented via memory pointer rules, not convoluted cryptography.



### In demand

Over £30m of UKRI funding has been allocated to developing CHERI processors in the past 5 years.



### **UK designed**

Abides by UK and ISO / BS regulations and supports local growth.



### Vital for the future of computing

Will be necessary for IP protection, memory security and sovereignty in coming years, especially in edge computing and embedded systems.

### 4 revenues 1 Ecosystem

**SERVICES** 

### **WARP OEMs**

Custom instances of WARP architecture, which we license to partners and provide MPW services through our web dashboard and end-to-end team.





**WARP Ecosystem** 

### **Labyrinth Access Control**

Blockchain-hosted decentralised private access control application, using TOTP codes, meaning users are immutable, and all data is private.

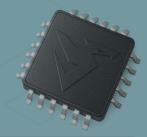




#### **PRODUCTS**

### WARP 2532 SoCs

In-house generic SoCs for developer boards and lowvolume industrial devices, support from our toolchain team comes part-and-parcel to integrate WARP into non-CHERI systems without compromise.



### **WARP Basilisk Storage**

Labyrinth-protected WARP-controlled secondary storage devices for impenetrable, access controlled, data storage.



### Don't Stick to the Status Quo





No current devices use CHERI commercially

This means memory is at risk and manufacturers don't have any choice.



### The Status Quo keeps the insecure chips around

No big chipmakers want to undermine the current market by introducing something revolutionary.



### WE provide the solution

WARP is the first commercially available CHERI enabled SoC in the world which can be customised for OEM applications.



### **Our OEM Process**





### Stage 1 Specification



Representatives of the company work with our engineering team to understand how WARP needs to be modified to integrate with their systems and vice versa.

Stage 2

### **Development**



Our engineering team is set to work adapting WARP to the OEM specification, ensuring each interface and system is secure.

Stage 3

### **Testing**



We provide custom FPGA boards for integration tests with your systems prior to our MPW runs or licensing to rule out bugs and compatibility issues.

Stage 4

### **Procurement**



Either licenses are provided for internal chip sourcing, or we will provide MPW services through our industry connections and handle all logistics up to SoC handover, including storage and distribution. Depending on volumes we can also arrange long-term shuttle agreements.



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